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APPLICATION FOR LETTERS PATENT

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Semiconductor Processing Methods Of Forming A
Conductive Projection And Methods Of Increasing
Alignment Tolerances

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1 SEMICONDUCTOR PROCESSING METHODS OF FORMING A
2 CONDUCTIVE PROJECTION AND METHODS OF INCREASING
3 ALIGNMENT TOLERANCES

4 TECHNICAL FIELD

5 This invention relates to semiconductor processing methods of
6 forming conductive projections, and to methods of increasing alignment
7 tolerances.

8
9 BACKGROUND OF THE INVENTION

10 As dimensions of semiconductor devices continue to shrink,
11 alignment of individual device components, and compensation for
12 misalignment become increasingly important. Problems associated with
13 feature misalignment can cause shorting and other catastrophic device
14 failure.

15 In forming semiconductor devices, it is not uncommon to use a
16 conductive projection of material such as a conductive plug to form an
17 intermediate electrical connection between a substrate node location and
18 a device component. An exemplary conductive projection is shown in
19 Figs. 1-3.

20 Referring to Fig. 1, a semiconductor wafer fragment is shown
21 generally at 20 and comprises a semiconductive substrate 22. In the
22 context of this document, the term "semiconductive substrate" is defined
23 to mean any construction comprising semiconductive material, including,
24 but not limited to, bulk semiconductive materials such as a

1 semiconductor wafer (either alone or in assemblies comprising other
2 materials thereon), and semiconductor material layers (either alone or
3 in assemblies comprising other materials). The term "substrate" refers
4 to any supporting structure, including, but not limited to, the
5 semiconductor substrates described above.

6 A pair of isolation oxide regions 24 are formed over substrate 22.
7 A plurality of conductive lines 26 are provided and typically include a
8 polysilicon layer 28, a silicide layer 30 and an insulative cap 32.
9 Sidewall spacers 34 are provided over conductive and non-conductive
10 portions of line 26. Diffusion regions 35 are provided and constitute
11 node locations with which electrical communication is desired. Wafer
12 fragment 20 comprises a portion of a dynamic random access memory
13 (DRAM) device. Conductive projections 36 are provided. A centermost
14 of the conductive projections 36 is positioned to establish electrical
15 communication between diffused regions and a bit line yet to be
16 formed. The conductive projections are typically formed within an
17 opening in an insulative oxide layer such as borophosphosilicate glass
18 (BPSG), and subsequently planarized. A layer 38 is formed over
19 substrate 22 and comprises an insulative material such as BPSG.

20 Referring to Fig. 2, a pair of contact openings 40 are formed
21 through layer 38 and outwardly expose the illustrated projections 36.
22 Contact openings 40 constitute openings within which storage capacitors
23 are to be formed. Such capacitors are typically formed by providing
24 a layer of conductive material within opening 40 and over layer 38, and

1 subsequently depositing a capacitor dielectric layer and cell plate layer
2 thereover.

3 Referring to Fig. 3, an enlarged portion of Fig. 2 shows an
4 example alignment tolerance X between centermost conductive
5 projection 36 and a dashed extension of the right edge of one
6 opening 40. A misalignment of the mask used to form contact
7 opening 40 which is greater than X, and in the direction of the
8 conductive projection, can result in overlap of contact opening 40 and
9 centermost conductive projection 36. Such would subsequently cause
10 conductive capacitor material provided into contact opening 40 to be
11 shorted with centermost conductive projection 36 thereby rendering this
12 portion of the device inoperative.

13 This invention arose out of concerns associated with increasing
14 alignment tolerances between conductive projections and electrical
15 components formed over a semiconductor wafer. The artisan will
16 appreciate other applicability, with the invention only being limited by
17 the accompanying claims appropriately interpreted in accordance with the
18 doctrine of equivalents.

19 20 SUMMARY OF THE INVENTION

21 Semiconductor processing methods of forming conductive projections
22 and methods of increasing alignment tolerances are described. In one
23 implementation, a conductive projection is formed over a substrate
24 surface area and includes an upper surface and a side surface joined

therewith to define a corner region. The corner region of the
conductive projection is subsequently beveled to increase an alignment
tolerance relative thereto. In another implementation, a conductive plug
is formed over a substrate node location between a pair of conductive
lines and has an uppermost surface. Material of the conductive plug
is unevenly removed to define a second uppermost surface, at least a
portion of which is disposed elevationally higher than a conductive line.
In one aspect, conductive plug material can be removed by facet etching
the conductive plug. In another aspect, conductive plug material is
unevenly doped with dopant, and conductive plug material containing
greater concentrations of dopant is etched at a greater rate than plug
material containing lower concentrations of dopant.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with
reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer
fragment in process in accordance with prior art methods.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing
step subsequent to that shown in Fig. 1.

Fig. 3 is an enlarged view of a portion of Fig. 2.

Fig. 4 is a view of a semiconductor wafer fragment in process in
accordance with one embodiment of the invention.

1 Fig. 5 is a view of the Fig. 4 wafer fragment at a processing
2 step subsequent to that shown in Fig. 4.

3 Fig. 6 is a view of the Fig. 4 wafer fragment at a processing
4 step subsequent to that shown in Fig. 5.

5 Fig. 7 is a view of the Fig. 4 wafer fragment at a processing
6 step subsequent to that shown in Fig. 6.

7 Fig. 8 is a view of the Fig. 4 wafer fragment at a processing
8 step subsequent to that shown in Fig. 7.

9 Fig. 9 is a view of the Fig. 4 wafer fragment at a processing
10 step subsequent to that shown in Fig. 8.

11 Fig. 10 is a view of the Fig. 4 wafer fragment at a processing
12 step subsequent to that shown in Fig. 9.

13 Fig. 11 is a view of the Fig. 4 wafer fragment at a processing
14 step subsequent to that shown in Fig. 10.

15 Fig. 12 is a view of the Fig. 10 wafer fragment at a processing
16 step in accordance with another embodiment of the invention.

17 Fig. 13 is a view of the Fig. 12 wafer fragment at a processing
18 step subsequent to that shown in Fig. 12.

19 Fig. 14 is a view of either of the Figs. 11 or 13 wafer fragments,
20 at a processing step subsequent to that shown in either of the
21 respective figures.

22 Fig. 15 is a view of the Fig. 14 wafer fragment at a processing
23 step subsequent to that shown in Fig. 14.
24

Fig. 16 is a view of the Fig. 14 wafer fragment at a processing step subsequent to that shown in Fig. 15.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 4, a semiconductor wafer fragment in process in accordance with one embodiment of the invention is shown generally at 42 and comprises a semiconductive substrate 44. A pair of conductive lines 46 are formed over substrate 44 and comprise a polysilicon layer 48, a silicide layer 50 and an insulative cap 52. Sidewall spacers 54 are provided over conductive and non-conductive portions of lines 46. Lines 46 constitute a pair of spaced-apart, insulated conductive lines which define a node location 56 or surface area therebetween with which electrical communication is desired. In the illustrated and preferred embodiment, node location 56 comprises a diffusion region 57 to be connected with a bit line. Other node locations are defined by diffusion regions 57 laterally outward of node location 56, and comprise locations with which electrical communication with storage capacitors is desired, as will become apparent below. A first insulative layer 58 is formed over node location 56 and between the conductive lines. An exemplary material for layer 58 is BPSG.

1 Referring to Fig. 5, layer 58 is planarized as by chemical
2 mechanical polishing to provide a generally planar upper surface 60.
3 The planarization of layer 58 can be made to stop on or over the
4 insulative caps of the conductive lines.

5 Referring to Fig. 6, a second layer of insulative material 62 is
6 formed over node location 56 and has a generally planar upper
7 surface 64.

8 Referring to Fig. 7, a patterned masking layer 66 is formed over
9 substrate 44.

10 Referring to Fig. 8, openings 68 are formed through material of
11 both first and second layers 58, 62 to proximate the node locations.
12 Preferably, the openings are sufficient to expose the node locations over
13 which each is formed.

14 Referring to Fig. 9, conductive material 70 is formed over the
15 substrate, insulative material 62, and within openings 68. The openings
16 are preferably filled with conductive material. An exemplary conductive
17 material is polysilicon.

18 Referring to Fig. 10, conductive material 70 is planarized relative
19 to insulative layer upper surface 64. Such isolates conductive material
20 within openings 68 and provides planarized conductive projections 72
21 over the substrate. In the illustrated and preferred embodiment,
22 conductive projections 72 constitute conductive plugs which are formed
23 in connection with formation of DRAM circuitry. Individual conductive
24 projections 72 include respective upper or uppermost surfaces 74 which

are joined with respective side surfaces 76. The side surfaces project away from the node location over which each is formed and terminate proximate the respective surface 74 with which it joins. Joinder between upper and side surfaces 74, 76 defines corner regions of the individual conductive projections. Intermediate and away from the corner regions of each projection is a central region 78.

Preferably and as shown, the individual conductive plugs project away from the respective node locations over which each is formed a distance which is further than a distance that one of the conductive lines projects away from the node location. Accordingly, each plug's uppermost surface is disposed elevationally over both conductive lines and is substantially coplanar with the generally planar portion of insulative material 62.

Referring to Fig. 11, corner regions of the conductive projections are beveled. In the illustrated example, the beveling of the corner regions comprises facet etching the conductive projection to provide the illustrated beveled construction. Such etching can take place in a cold wall processing chamber using an unheated chuck. Other conditions include a power setting of between 100 W to 600 W, a pressure setting of between 10 to 100 mTorr, and use of Argon ions preferably having incident angles of between 45° to 60°. The insulative material can be removed prior to the facet etching. Alternately, the insulative material can remain during the facet etching.

1 The facet etching of the conductive projection constitutes unevenly
2 removing the conductive material sufficient to define a second uppermost
3 surface 80, at least of portion of which is disposed elevationally higher
4 than the conductive lines. In this example, more material is removed
5 from the corner region than from the central region of each plug, and
6 second uppermost surface 80 is generally non-planar.

7 Referring to Fig. 12, a second embodiment is shown, with the
8 discussion proceeding with processing subsequent to the Fig. 10 wafer
9 fragment. In this example, the conductive projections are unevenly
10 doped proximate the upper and side surfaces. Such uneven doping can
11 be accomplished using an angled ion implant at energies between
12 about 20 keV to 1000 keV, and angles greater than 0° and less than
13 about 60°. The angled ion implant subjects the corner regions to a
14 greater degree of normal angle implanting such that greater implanting
15 occurs relative to the corner regions as opposed to the upper surfaces.
16 As a result, outermost side portions, e.g. the corner regions, of the
17 conductive plug have greater concentrations of dopant than plug material
18 therebetween proximate the central region. Insulative material 62
19 (Fig. 10) can be removed prior to doping the conductive plugs, or
20 remain during the doping.

21 Referring to Fig. 13, the individual conductive plugs have been
22 beveled. Such can be accomplished by etching material of the
23 conductive plugs or projections containing greater concentrations of
24 dopant at a greater rate than material of the conductive projections

1 containing lower concentrations of dopant. Insulative material 62
2 (Fig. 10) can be removed prior to the etching of the conductive plugs
3 or remain during the etching. The beveling of the conductive plugs
4 comprises unevenly removing material of the conductive plug to define
5 a second uppermost surface 80a, at least a portion of which is disposed
6 elevationally higher than the conductive lines. Exemplary etching can
7 comprise dry or wet etching of the plug material. In the former, Cl_2
8 or HBr chemistries can be used to sufficiently activate etching of the
9 corner regions. In the latter, wet etches with a sufficiently high pH can
10 be used. Examples include TMAH or SCI (APM).

11 Referring to Fig. 14, a layer of material 82 is formed over the
12 substrate, with BPSG being but one example.

13 Referring to Fig. 15, openings 84 are formed over the substrate
14 and define a second alignment tolerance X_1 which is greater than the
15 first alignment tolerance X (Fig. 3).

16 Referring to Fig. 16, conductive material 86 has been formed
17 over, and is in electrical communication with the leftmost and rightmost
18 conductive plugs and the respective diffusion regions over which the
19 plugs are formed. Conductive material 86 constitutes respective storage
20 node layers. Dielectric layers 88 are formed over the respective storage
21 node layers 86, and a cell plate layer 90 is formed over the respective
22 dielectric layers. Conductive material 94 is formed over, and is in
23 electrical communication with the centermost conductive plug and the
24 diffusion region over which it is formed. Conductive material 94

1 comprises a bit line. Here, the alignment tolerance between bit line
2 contact material and adjacent storage capacitors is increased.

3 Advantages of the above-described methods and structures include
4 that alignment tolerances can be increased with only a slight
5 modification of the processing flow. Process viability can be improved
6 for shifts which may occur in or during photo alignment. Additionally,
7 the above methods allow scaling of contemporary technology to smaller
8 generations of devices.

9 In compliance with the statute, the invention has been described
10 in language more or less specific as to structural and methodical
11 features. It is to be understood, however, that the invention is not
12 limited to the specific features shown and described, since the means
13 herein disclosed comprise preferred forms of putting the invention into
14 effect. The invention is, therefore, claimed in any of its forms or
15 modifications within the proper scope of the appended claims
16 appropriately interpreted in accordance with the doctrine of equivalents.
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